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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,538	11/07/2001	Luca Battu'	851763.420	2722

500 7590 09/20/2005

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EXAMINER	
PATEL, SHAMBHAVI K	

ART UNIT	PAPER NUMBER
2128	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,538	BATTU' ET AL.	
	Examiner	Art Unit	
	Shambhavi Patel	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/07/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Europe on 11/07/2000. It is noted, however, that applicant has not filed a certified copy of the 00830735.7 application as required by 35 U.S.C. 119(b).

Information Disclosure Statement

The information disclosure statement filed 11/07/01 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each cited foreign patent document; each non-patent literature publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Allen et al (US Patent No. 6,151,568), herein referred to as Allen.

4. As per claim 1, Allen is directed to a process for estimating power consumption (column 1 lines 7-8) over a given time interval (column 10 line 51) of digital circuits (column 2 lines 26-27) described at the level of simulated functional elements (column 1 lines 8-11) provided with input/output terminals (column 3 lines 64-67, column 4 line 1), characterized in that it comprises the operations of:

a. Emulating, at the hardware level (column 4 lines 7-11, lines 26-34), additional elements associated to said functional elements; said additional emulated elements being able to detect, during emulation of the circuit, at least one signal indicative of the behavior, and hence of power consumption, of the corresponding functional element associated during said time interval (column 2 lines 33–39). The examiner interprets the statement "emulating at the hardware level" to mean running a simulation on any hardware peripheral. Allen's invention discloses a simulation software that is to be run on a computer (column 5 lines 18-22).

b. Acquiring the value of said at least one signal, said value being indicative of the power consumption of said associated functional element in said given time interval (column 2 lines 55-61).

5. As per claim 2, Allen is directed to the process according to claim 1, wherein said additional elements are emulated by associating them to an output of the respective functional element (column 9 lines 47-57).

6. As per claim 3, Allen is directed to the process according to claim 1, wherein said additional emulated elements are able to detect, during said given time interval:

c. The number of transitions performed by the corresponding associated functional element (column 10 lines 25-36); and

d. The fraction of time in which the state of the corresponding associated functional element is stable (column 10 lines 38-40). The Illustrated Dictionary of Electronics defines stability as "the condition in which an equipment or device is able to maintain a particular mode of operation without deviation" (Gibilisco 652). The examiner interprets "a particular mode of operation without deviation" to mean a state where the device is set high for a set period of time. Allen's discloses a process where the simulator measures the duty cycle, which is defined by the Illustrated Dictionary of Electronics as "the proportion of percentage of time during which a device, circuit, or system is operating or handling power" (Gibilisco 220). The examiner interprets "operating" to mean a state when the device is set high for a set period of time. Thus the duty cycle measured in Allen's invention and the stability measured in the claimed invention are equivalent.

e. The value of said number of transitions and said fraction of time being indicative of the power consumption of said functional element during said time interval (column 14 lines 7-10).

7. As per claim 4, Allen is directed to the process according to claim 1, wherein it comprises the operation of controlling the acquisition of said at least one signal by means of hardware events monitored by logic analyzers active on the emulator (column 10 lines 25-36).

8. As per claim 5, Allen is directed to the process according to claim 1, wherein it comprises the operation of accessing the information stored in said additional emulated elements and the operation of storing said information (column 14 lines 28-30) in view of subsequent processing (column 4 lines 33-38).

9. As per claim 6, Allen is directed to a processing system configured for the implementation of the process according to claim 1 (column 5 lines 18-19).

10. As per claim 7, Allen is directed to a computer program product directly loadable into the internal memory of a digital computer, comprising software code portions for performing the steps of claim 1 when said product is run on a computer (column 2 lines 27-32).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Please see attached PTO-892.

f. Tan-Li Chou et al, Accurate Power Estimation of CMOS Sequential Circuits. September 1996, Volume 4, Issue 3; pages 369-380.

g. Najm, F.N; A Survey of Power Estimation Techniques in VLSI Circuits; Dec 1994, Volume 2, Issue 4; pages 446-455.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is 571 272 5877. The examiner can normally be reached on 7:30 am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached on (571)272-3780. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JEAN R. HOMERE
PRIMARY EXAMINER